WE CLAIM:

1. A common mode linearized input stage, comprising:

a differential input terminal V_{in+};

a differential input terminal V_{in-}, said differential input terminals connected to receive a differential input signal;

first and second NPN transistors arranged as a differential transistor pair, the bases of said first and second NPN transistors connected to V_{in+} and V_{in-}, respectively, the emitters of said first and second NPN transistors connected together at a first node, and the collectors of said first and second NPN transistors conducting respective currents I_{D1+} and I_{D1-} in response to said differential input signal;

first and second PNP transistors arranged as a differential transistor pair, the bases of said first and second PNP transistors connected to V_{in-} and V_{in+}, respectively, the emitters of said first and second PNP transistors connected together at a second node, and the collectors of said first and second PNP transistors conducting respective currents I_{D2+} and I_{D2-} in response to said differential input signal;

a first tail current source connected to said first node to provide a first tail current I_{tail1} to said NPN differential transistor pair;

a second tail current source connected to said second node to provide a second tail current I_{tail2} to said PNP differential transistor pair; and

a tail current modulation circuit which generates complementary output currents I_{in1}, I_{in2} as a function of the difference between the voltages at said first and second nodes;

said first tail current source arranged to generate said first tail current I_{tail1} as a function of I_{in1}, and said second tail current source arranged to generate said second tail current I_{tail2} as a function of I_{in2}, said tail current modulation circuit and said first and second tail current sources arranged such that the magnitudes of tail currents I_{tail1} and I_{tail2} increase with an increasing differential input signal.

2. The input stage of claim 1, wherein said tail current modulation circuit comprises:

a PNP diversion transistor having its base connected to said first node, its collector coupled to said first tail current source, and its emitter connected to a third node; and

a NPN diversion transistor having its base connected to said second node, its collector coupled to said second tail current source, and its emitter connected to said third node,

said PNP and NPN diversion transistors conducting complementary output currents I_{in1} and I_{in2}, respectively.

3. The input stage of claim 1, wherein the transistors comprising said NPN and PNP differential transistors pairs each have an emitter size of 1, and said NPN and PNP diversion transistors each have an emitter size of A, such that, when fully conducting, said PNP and NPN diversion transistors reduce said first and second tail currents by a scaling ratio of A.

4. A common mode linearized input stage, comprising:

a differential input terminal V_{in+};

a differential input terminal V_{in-}, said differential input terminals connected to receive a differential input signal;

first and second NPN transistors arranged as a differential transistor pair, the bases of said first and second NPN transistors connected to V_{in+} and V_{in-}, respectively, the emitters of said first and second NPN transistors connected together at a first node, and the collectors of said first and second NPN transistors conducting respective currents I_{D1+} and I_{D1-} in response to said differential input signal;

first and second PNP transistors arranged as a differential transistor pair, the bases of said first and second PNP transistors connected to V_{in-} and V_{in+}, respectively, the emitters of said first and second PNP transistors connected together at a second node, and the collectors of said first and second PNP transistors conducting respective currents I_{D2+} and I_{D2-} in response to said differential input signal;

a first tail current source connected to said first node to provide a first tail current I_{tail1} to said NPN differential transistor pair;

a second tail current source connected to said second node to provide a second tail current I_{tail2} to said PNP differential transistor pair;

a PNP diversion transistor having its base connected to said first node, its collector coupled to said first tail current source, and its emitter connected to a third node; and

a NPN diversion transistor having its base connected to said second node, its collector coupled to said second tail current source, and its emitter connected to said third node, such that said PNP and NPN diversion transistors conduct complementary output currents I_{in1} and I_{in2}, respectively, as a function of the difference between the voltages at said first and second nodes;

said first tail current source arranged to generate I_{tail1} as a function of I_{in1} and said second tail

current source arranged to generate I_{tail2} as a function of I_{in2}, such that the magnitudes of I_{tail1} and I_{tail2} increase with an increasing differential input signal.

5. The input stage of claim 4, wherein the transistors comprising said NPN and PNP differential transistors pairs each have an emitter size of 1, and said NPN and PNP diversion transistors each have an emitter size of A, such that, when fully conducting, said PNP and NPN diversion transistors reduce said first and second tail currents by a scaling ratio of A.

6. The input stage of claim 5, wherein the values of I_{tail1} and I_{tail2} when said PNP and NPN diversion transistors are off are equal to $I_{1(max)}$ and $I_{2(max)}$, respectively, and said input stage is arranged such that the current I_{D1+} conducted by said first NPN transistor is given by:

$$I_{D1+} = \frac{e^{\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{1(max)}$$

the current conducted by said second NPN transistor is given by:

$$I_{D1-} = \frac{e^{-\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{1(max)}$$

and the current I_{div} conducted by said PNP and NPN diversion transistors is given by:

$$I_{div} = \frac{A}{e^{\alpha} + A + e^{-\alpha}}$$

where α is given by:

$\alpha = \frac{V_{in+} - V_{in-}}{2 * V_t}$, where V_t is the thermal voltage $\frac{kT}{q}$,

and the transconductance G_m of the input stage is given by:

$$G_m = \frac{2A * \cosh\alpha + 4}{(2 * \cosh\alpha + A)^2} \bullet \frac{d\alpha}{d(V_{in+} - V_{in-})} \bullet I_{(max)}$$

assuming $I_{1(max)} = I_{2(max)} = I_{(max)}$.

7. The input stage of claim 5, wherein the value of A is selected such that G_m increases with the magnitude of said differential input signal.

8. The input stage of claim 5, wherein the value of A is selected to linearize the response of said NPN and PNP differential transistor pairs.

9. The input stage of claim 5, wherein the value of A is selected to provide a transconductance G_m for said input stage that decompresses said differential input signal.

10. The input stage of claim 9, further comprising a following stage which receives said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-} and produces an output current in response, said following stage having an associated compression characteristic such that said output current does not vary linearly with said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-}, wherein the value of A is selected to provide a transconductance G_m for said input stage that decompresses said differential input signal so as to compensate for said following stage's compression.

11. The input stage of claim 5, wherein the value of A is at least four.

12. The input stage of claim 4, wherein said first tail current source comprises:

a first fixed current source connected to provide a first output current at a fourth node; and

a first bias transistor having its current circuit connected between said first node and said fourth node and biased to conduct at least a portion of said first output current as said first tail current I_{tail1}, the

collector of said PNP diversion transistor coupled to said fourth node such that I_{tail1} is reduced when said PNP diversion transistor is conducting;

and said second tail current source comprises:

a second fixed current source connected to provide a second output current at a fifth node; and

a second bias transistor having its current circuit connected between said second node and said fifth node and biased to conduct at least a portion of said second output current as said second tail current I_{tail2}, the collector of said NPN diversion transistor coupled to said fifth node such that I_{tail2} is reduced when said NPN diversion transistor is conducting.

13. The input stage of claim 12, wherein said first and second fixed current sources are first and second resistors, respectively.

14. The input stage of claim 4, wherein said first tail current source comprises:

a first fixed current source connected to provide a first output current; and

a first current mirror connected to mirror said first output current to said first node such that at least a portion of said first output current is provided as said first tail current I_{tail1}, said first current mirror comprising:

a first diode-connected input transistor connected to receive said first output current, and

a first output transistor having its base connected to the base of said first diode-connected transistor at a fourth node and its emitter connected to said first diode-connected transistor's emitter such that said first output current is mirrored to said first node and said first output transistor conducts said first tail

current I_{tail1}; and

a second current mirror, comprising:

a second diode-connected input transistor coupled to the collector of said PNP diversion transistor, and

a second output transistor connected to mirror the current in said PNP diversion transistor to said fourth node such that I_{tail1} is reduced when said PNP diversion transistor is conducting; and

said second tail current source comprises:

a third current mirror connected to mirror said first output current to said second node such that at least a portion of said first output current is provided as said second tail current I_{tail2}, said third current mirror comprising:

a third diode-connected input transistor connected to receive said first output current, and

a third output transistor having its base connected to the base of said third diode-connected transistor at a fifth node and its emitter connected to said third diode-connected transistor's emitter such that said first output current is mirrored to said second node and said third output transistor conducts said second tail current I_{tail2}; and

a fourth current mirror, comprising:

a fourth diode-connected input transistor coupled to the collector of said NPN diversion transistor, and

a fourth output transistor connected to mirror the current in said NPN diversion transistor to said fifth node such that I_{tail2} is reduced when said NPN diversion transistor is conducting.

15. The input stage of claim 4, wherein said input stage is arranged such that said PNP and NPN diversion

transistors are off when said input stage is slewing in response to a changing differential input signal.

16. The input stage of claim 4, further comprising a input stage mirroring structure connected between first and second supply voltages and which receives said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-} and produces an output current in response, said input stage mirroring structure comprising:

a first current mirror circuit having an input and output, said differential output currents I_{D1+} and I_{D1-} coupled to first current mirror circuit at fourth and fifth nodes, respectively, said first current mirror circuit arranged such that I_{D1+} and I_{D1-} inject offset current into an otherwise balanced current mirror such that the current at said first current mirror circuit's output varies only when I_{D1+} and I_{D1-} are unequal;

a second current mirror circuit having an input and output and complementary to said first current mirror circuit, said differential output currents I_{D2+} and I_{D2-} coupled across said second current mirror circuit at sixth and seventh nodes, respectively, said second current mirror circuit arranged such that I_{D2+} and I_{D2-} inject offset current into an otherwise balanced current mirror such that the current at said second current mirror circuit's output varies only when I_{D2+} and I_{D2-} are unequal;

a single floating current source connected between the inputs of said first and second current mirror circuits, the outputs of said first and second current mirror circuits coupled to an output node, the current at said output node being said output current;

such that noise due to said floating current source is correlated for the two current mirror circuits such that said noise sums to zero at said output node, said input stage connected to said mirroring structure in a balanced fashion such that a change in I_{tail1}

shifts the voltages at said fourth and fifth nodes by equal amounts and a change in I_{tail2} shifts the voltages at said sixth and seventh nodes by equal amounts without changing said output current, thereby rejecting common mode noise.

17. The input stage of claim 16, wherein said floating current source comprises:

an NPN transistor;

a PNP transistor;

a resistor, the emitter of said NPN transistor connected in series with the emitter of said PNP transistor via said resistor;

a first reference voltage connected between the bases of said NPN and PNP transistors; and

a second reference voltage connected between ground and the base of said PNP transistor;

such that said NPN and PNP transistors conduct said bias current I_{bias}.

18. The input stage of claim 16, further comprising a compensation capacitor connected between said output node and one of said supply voltages.

19. The input stage of claim 16, further comprising a buffer stage connected at its input to said output node and providing a buffered version of said output current at its output.

20. The input stage of claim 16, wherein the transistors comprising said NPN and PNP differential transistor pairs each have an emitter size of 1, and said NPN and PNP diversion transistors each have an emitter size of A, such that said PNP and NPN diversion transistors conduct and thereby divert said first and second tail currents by a scaling ratio of A when said differential

input signal is zero, wherein the value of A is selected to provide a transconductance G_m for said input stage that decompresses said differential input signal.

21. The input stage of claim 20, wherein said input stage mirroring structure has an associated compression characteristic such that said output current does not vary linearly with said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-}, wherein the value of A is selected to provide a transconductance G_m for said input stage that decompresses said differential input signal so as to compensate for said input stage mirroring structure's compression.

22. The input stage of claim 4, further comprising a input stage mirroring structure connected between first and second supply voltages and which receives said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-} and produces an output current in response, said input stage mirroring structure comprising:

first and second degeneration resistors connected between said first supply voltage and fourth and fifth nodes, respectively, said currents I_{D1+} and I_{D1-} connected to said fourth and fifth nodes, respectively;

third and fourth degeneration resistors connected between said second supply voltage and sixth and seventh nodes, respectively, said currents I_{D2+} and I_{D2-} connected to said sixth and seventh nodes, respectively;

a first current mirror connected between said fourth and fifth nodes, comprising:

a first diode-connected input transistor having its emitter connected to said fifth node,

a first current mirror output transistor having its emitter connected to said fourth node, the bases of said first current mirror transistors connected together;

a second current mirror connected between said

sixth and seventh nodes, comprising:

a second diode-connected input transistor having its emitter connected to said sixth node,

a second current mirror output transistor having its emitter connected to said seventh node, the bases of said second current mirror transistors connected together;

a bias current source connected between the collector of said first current mirror output transistor at an eighth node and the collector of said second current mirror output transistor at a ninth node;

an output node;

a PNP output transistor having its base connected to said eighth node, its emitter connected to the collector of said first diode-connected input transistor, and its collector connected to said output node; and

a NPN output transistor having its base connected to said ninth node, its emitter connected to the collector of said second diode-connected input transistor, and its collector connected to said output node,

the current at said output node being said output current.

23. The input stage of claim 4, further comprising a input stage mirroring structure connected between first and second supply voltages and which receives said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-} and produces an output current I_{out} in response, said input stage mirroring structure comprising:

first and second degeneration resistors connected between said first supply voltage and fourth and fifth nodes, respectively;

third and fourth degeneration resistors connected between said second supply voltage and sixth and seventh nodes, respectively;

a first current mirror circuit connected between

said fourth and fifth nodes, comprising:

a first diode-connected input transistor having its emitter connected to said fifth node,

a first current mirror output transistor having its emitter connected to said fourth node, the bases of said first current mirror transistors connected together;

a second current mirror connected between said sixth and seventh nodes, comprising:

a second diode-connected input transistor having its emitter connected to said sixth node,

a second current mirror output transistor having its emitter connected to said seventh node, the bases of said second current mirror transistors connected together;

a third diode-connected transistor having its emitter connected to the collector of said first current mirror output transistor at an eighth node and its base and collector connected together;

a fourth diode-connected transistor having its emitter connected to the collector of said second current mirror output transistor at a ninth node and its base and collector connected together;

a bias current source connected between the collector of said third diode-connected transistor and the collector of said fourth diode-connected transistor;

an output node;

a PNP output transistor having its base connected to the base and collector of said third diode-connected transistor, its emitter connected to the collector of said first diode-connected input transistor at a tenth node, and its collector connected to said output node; and

a NPN output transistor having its base connected to the base and collector of said fourth diode-connected transistor, its emitter connected to the collector of said

second diode-connected input transistor at an eleventh node, and its collector connected to said output node;

said currents I_{D1+} and I_{D1-} connected to said eighth and tenth nodes, respectively;

said currents I_{D2+} and I_{D2-} connected to said eleventh and ninth nodes, respectively;

the current at said output node being said output current, said input stage mirroring structure arranged such that I_{out} is given by:

$I_{out} = I_{D2+} + I_{D1+} - I_{D2-} - I_{D1-}$.

24. A common mode linearized input stage, comprising:

a differential input terminal V_{in+},

a differential input terminal V_{in-}, said differential input terminals connected to receive a differential input signal;

first and second NPN transistors arranged as a differential transistor pair, the bases of said first and second NPN transistors connected to V_{in+} and V_{in-}, respectively, the emitters of said first and second NPN transistors connected together at a first node, and the collectors of said first and second NPN transistors conducting respective currents I_{D1+} and I_{D1-} in response to said differential input signal;

first and second PNP transistors arranged as a differential transistor pair, the bases of said first and second PNP transistors connected to V_{in-} and V_{in+}, respectively, the emitters of said first and second PNP transistors connected together at a second node, and the collectors of said first and second PNP transistors conducting respective currents I_{D2+} and I_{D2-} in response to said differential input signal,

said first and second NPN transistors and said first and second PNP transistors each having an emitter size of 1;

a first tail current source connected to said first node to provide a first tail current I_{tail1} to said NPN differential transistor pair;

a second tail current source connected to said second node to provide a second tail current I_{tail2} to said PNP differential transistor pair;

a PNP diversion transistor having its base connected to said first node, its collector coupled to said first tail current source, and its emitter connected to a third node; and

a NPN diversion transistor having its base connected to said second node, its collector coupled to said second tail current source, and its emitter connected to said third node, said PNP and NPN diversion transistors each having an emitter size of A,

such that said PNP and NPN diversion transistors conduct and thereby divert said first and second tail currents from said NPN and PNP differential transistor pairs by a scaling ratio of A when said differential input signal is zero;

said input stage arranged such that the current I_{D1+} conducted by said first NPN transistor is given by:

$$I_{D1+} = \frac{e^{\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{1(max)}$$

the current conducted by said second NPN transistor is given by:

$$I_{D1-} = \frac{e^{-\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{1(max)}$$

and the current I_{div} conducted by said PNP and NPN diversion transistors is given by:

$$I_{div} = \frac{A}{e^{\alpha} + A + e^{-\alpha}}$$

where α is given by:

$\alpha = \frac{V_{in+} - V_{in-}}{2 * V_t}$, where V_t is the thermal voltage $\frac{kT}{q}$, and the transconductance G_m of the input stage is given by:

$$G_m = \frac{2A * \cosh\alpha + 4}{(2 * \cosh\alpha + A)^2} \bullet \frac{d\alpha}{d(V_{in+} - V_{in-})} \bullet I_{(max)}$$

assuming $I_{1(max)} = I_{2(max)} = I_{(max)}$.

25. The input stage of claim 24, further comprising a input stage mirroring structure connected between first and second supply voltages and which receives said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-} and produces an output current in response, said input stage mirroring structure comprising:

first and second degeneration resistors connected between said first supply voltage and fourth and fifth nodes, respectively, said currents I_{D1+} and I_{D1-} connected to said fourth and fifth nodes, respectively;

third and fourth degeneration resistors connected between said second supply voltage and sixth and seventh nodes, respectively, said currents I_{D2+} and I_{D2-} connected to said sixth and seventh nodes, respectively;

a first current mirror connected between said fourth and fifth nodes, comprising:

a first diode-connected input transistor having its emitter connected to said fifth node,

a first current mirror output transistor having its emitter connected to said fourth node, the bases of said first current mirror transistors connected together;

a second current mirror connected between said sixth and seventh nodes, comprising:

a second diode-connected input transistor having its emitter connected to said sixth node,

a second current mirror output transistor having its emitter connected to said seventh node, the

bases of said second current mirror transistors connected together;

a bias current source connected between the collector of said first output transistor at an eighth node and the collector of said second output transistor at a ninth node;

an output node;

a PNP output transistor having its base connected to said eighth node, its emitter connected to the collector of said first diode-connected input transistor, and its collector connected to said output node; and

a NPN output transistor having its base connected to said ninth node, its emitter connected to the collector of said second diode-connected input transistor, and its collector connected to said output node,

the current at said output node being said output current.

26. The input stage of claim 25, wherein said input stage mirroring structure has an associated compression characteristic such that said output current does not vary linearly with said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-}, wherein the value of A is selected to provide a transconductance G_m for said input stage that decompresses said differential input signal so as to compensate for said input stage mirroring structure's compression.

27. A common mode linearized input stage, comprising:

first and second supply voltages;

a differential input terminal V_{in+};

a differential input terminal V_{in-}, said differential input terminals connected to receive a differential input signal;

first and second NPN transistors arranged as a differential transistor pair, the bases of said first and

second NPN transistors connected to V_{in+} and V_{in-}, respectively, the emitters of said first and second NPN transistors connected together at a first node, and the collectors of said first and second NPN transistors conducting respective currents in response to said differential input signal;

first and second PNP transistors arranged as a differential transistor pair, the bases of said first and second PNP transistors connected to V_{in-} and V_{in+}, respectively, the emitters of said first and second PNP transistors connected together at a second node, and the collectors of said first and second PNP transistors coupled to said second supply voltage;

a first tail current source connected between said first node and said second supply voltage to provide a first tail current I_{tail1} to said NPN differential transistor pair;

a second tail current source connected between said first supply voltage and said second node to provide a second tail current I_{tail2} to said PNP differential transistor pair;

a PNP diversion transistor having its base connected to said first node, its collector coupled to said first tail current source, and its emitter connected to a third node; and

a NPN diversion transistor having its base connected to said second node, its collector coupled to said first supply voltage, and its emitter connected to said third node,

such that said PNP and NPN diversion transistors conduct and thereby divert said first tail current from said NPN differential transistor pair when said differential input signal is zero.

28. An amplifier, comprising:

an input stage; and

an input stage mirroring structure;

said input stage comprising:

a differential input terminal V_{in+};

a differential input terminal V_{in-}, said differential input terminals connected to receive a differential input signal;

first and second NPN transistors arranged as a differential transistor pair, the bases of said first and second NPN transistors connected to V_{in+} and V_{in-}, respectively, the emitters of said first and second NPN transistors connected together at a first node, and the collectors of said first and second NPN transistors conducting respective currents I_{D1+} and I_{D1-} in response to said differential input signal;

first and second PNP transistors arranged as a differential transistor pair, the bases of said first and second PNP transistors connected to V_{in-} and V_{in+}, respectively, the emitters of said first and second PNP transistors connected together at a second node, and the collectors of said first and second PNP transistors conducting respective currents I_{D2+} and I_{D2-} in response to said differential input signal;

a first tail current source connected to said first node to provide a first tail current I_{tail1} to said NPN differential transistor pair;

a second tail current source connected to said second node to provide a second tail current I_{tail2} to said PNP differential transistor pair;

a tail current modulation circuit which generates complementary output currents I_{in1}, I_{in2} as a function of the difference between the voltages at said first and second nodes;

said first tail current source arranged to generate said first tail current I_{tail1} as a function of I_{in1},

and said second tail current source arranged to generate said second tail current I_{tail2} as a function of I_{in2}, said tail current modulation circuit and said first and second tail current sources arranged such that the magnitudes of tail currents I_{tail1} and I_{tail2} increase with an increasing differential input signal;

said input stage mirroring structure connected between first and second supply voltages and which receives said currents I_{D1+}, I_{D1-}, I_{D2+} and I_{D2-} and produces an output current in response, said input stage mirroring structure comprising:

a first current mirror circuit having an input and output, said differential output currents I_{D1+} and I_{D1-} coupled to first current mirror circuit at third and fourth nodes, respectively, said first current mirror circuit arranged such that I_{D1+} and I_{D1-} inject offset current into an otherwise balanced current mirror such that the current at said first current mirror circuit's output varies only when I_{D1+} and I_{D1-} are unequal;

a second current mirror circuit having an input and output and complementary to said first current mirror circuit, said differential output currents I_{D2+} and I_{D2-} coupled to second current mirror circuit at fifth and sixth nodes, respectively, said second current mirror circuit arranged such that I_{D2+} and I_{D2-} inject offset current into an otherwise balanced current mirror such that the current at said second current mirror circuit's output varies only when I_{D2+} and I_{D2-} are unequal;

a single floating current source connected between the inputs of said first and second current mirror circuits, the outputs of said first and second current mirror circuits coupled to an output node, the current at said output node being said output current;

such that noise due to said floating current source is correlated for the two current mirror

circuits such that its noise sums to zero at said output node, said input stage connected to said mirroring structure in a balanced fashion such that a change in I_{tail1} shifts the voltages at said third and fourth nodes by equal amounts and a change in I_{tail2} shifts the voltages at said fifth and sixth nodes by equal amounts without changing said output current, thereby rejecting common mode noise.